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| Form PTO-1449 U.S. Department of Commerce<br>Patent and Trademark Office                      |  | Docket No.<br>D5116-00002         |  | Serial No.<br>09/675,427 |  |
| INFORMATION DISCLOSURE<br>STATEMENT<br>IN AN APPLICATION<br>(Use several sheets if necessary) |  | Applicant<br>Saxena et al.        |  |                          |  |
|   |  | Filing Date<br>September 29, 2000 |  | Group Art Unit<br>2812   |  |



| U.S. PATENT DOCUMENTS |                 |           |         |          |          |                                  |  |
|-----------------------|-----------------|-----------|---------|----------|----------|----------------------------------|--|
| *EXAMINER<br>INITIAL  | DOCUMENT NUMBER | DATE      | NAME    | CLASS    | SUBCLASS | FILING DATE<br>IF<br>APPROPRIATE |  |
| H.D.                  | AA              | 5,767,542 | 6/16/98 | Nakamura | 57       | 296                              |  |
| H.D.                  | AB              | 5,773,315 | 6/30/98 | Jarvis   | 438      | 14                               |  |
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| OTHER (Including Author, Title, Date, Pertinent Pages, Etc.) |   |   |
|--|---|---|
| H.D.   | A | International Search Report dated 09 APR 2001   |
| H.D.   | B | Khare et al., "Extraction of Defect Characteristics for Yield Estimation Using The Double Bridge Test Structure", IEEE, May 1991, pages 428-432               |
| H.D.   | C | Yun et al., "Evaluating the Manufacturability of GaAs/AlGaAs Multiple Quantum Well Avalanche Photodiodes Using Neural Networks, IEEE, Oct 1997, pages 105-112 |
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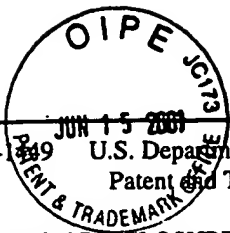
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| Form PTO-449<br><b>INFORMATION DISCLOSURE STATEMENT<br/>IN AN APPLICATION</b><br><br>(Use several sheets if necessary) | Docket No.<br>D5116-00002     | Serial No.<br>09/675,427 |
|  | Applicant<br>Saxena et al     |                          |
|  | Filing Date<br>Sept. 29, 2000 | Group Art Unit<br>2812   |

| U.S. PATENT DOCUMENTS |   |                 |          |               |       |          |                                  |
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| *EXAMINER<br>INITIAL  |   | DOCUMENT NUMBER | DATE     | NAME          | CLASS | SUBCLASS | FILING DATE<br>IF<br>APPROPRIATE |
| H.D.                  | A | 3,751,647       | 8/7/73   | Maeder et al. | 235   | 151.11   |                                  |
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| H.D.   | D | Khare et al., "Yield Oriented Computer-Aided Defect Diagnosis", IEEE Trans. on Semiconductor Manufacturing, Vol. 8, No. 02, May 1995 (02.05.1995), pages 195-206 |
| H.D.   | E | International Search Report dated 08 JUN 2001  |
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| EXAMINER  | <i>Harung-deu Day</i> | DATE CONSIDERED | 3/24/05 |
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Form PTO-1449 U.S. Department of Commerce  
Patent and Trademark OfficeDocket No.  
D5116-00002Serial No.  
09/675,427INFORMATION DISCLOSURE STATEMENT  
IN AN APPLICATIONApplicant  
Saxena et al.Filing Date  
November 29, 2000Group Art Unit  
2812

Use several sheets if necessary)

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| INITIAL |   | DOCUMENT NUMBER | DATE    | NAME        | CLASS | SUBCLASS | FILING DATE<br>IF<br>APPROPRIATE |
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| H.D.    | A | 4,835,466       | 5/30/89 | Maly et al. | 324   | 158R     |                                  |
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|  |  |                 |      |         |       |          |             |    |
|  |  |                 |      |         |       |          |             |    |

## OTHER (Including Author, Title, Date, Pertinent Pages, Etc.)

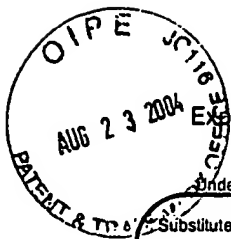
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| H.D. | B | Nurani et al., "In-Line Yield Prediction Methodologies Using Patterned Wafer Inspection Information", IEEE Transactions on Semiconductor Manufacturing, Vol. 11, No. 1, Feb 1998, pp.40-47 |  |  |  |  |  |  |
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|                        |                                      |
|------------------------|--------------------------------------|
| Application Number     | 09/675,427                           |
| Filing Date            | September 29, 2000 AUG 27 2004       |
| First Named Inventor   | Sharad Saxena Technology Center 2100 |
| Art Unit               | 2128                                 |
| Examiner Name          | Morella I Rosales Hanner             |
| Attorney Docket Number | D5116-00002                          |

Sheet 1 of 2

## NON PATENT LITERATURE DOCUMENTS

| Examiner Initials* | Cite No. <sup>1</sup> | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published. | T <sup>2</sup> |
|--------------------|-----------------------|---|----------------|
| H.D.               |                       | Y. CHENG et al., "MOSFET Modeling and BSIM User Guide." Kluwer Academic Publishers, Boston, 1999  | ✓              |
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| H.D.               |                       | "pdPCA User's Manual." Version 7, PDF Solutions, Inc., San Jose, 1998   |                |

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|--------------------|-------------------------|-----------------|---------|
| Examiner Signature | <i>Herring-De-De-De</i> | Date Considered | 3/24/05 |
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